CADSTAR

CADSTAR FPGA

D A T A S H E E T

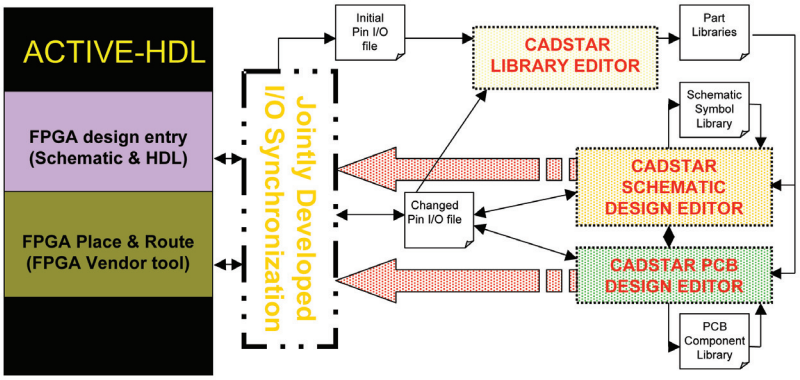
A new collaborative product, combining ACTIVE-HDL lite and CADSTAR in one universal project manager.

Complete FPGA - PCB design and verification

The FPGA technology offers today's electronic industry many advantages, like performance, time-to-market and cost reduction, but the increasing adoption of large, high-pin-count and high-speed FPGA devices means that right-first-time printed circuit board design practices are more essential than ever. This development forces the PCB design tools to provide solutions for the complete FPGA –PCB design and verification flow.

CADSTAR FPGA accommodates any combination of logic synthesis and intuitive implementation tools, giving the designer the freedom to use the tool of their choice to best meet the needs of each design.

CADSTAR FPGA allows the designers to easily integrate the FPGA design in the PCB board design. With the intuitive design flow manager, CADSTAR FPGA offers a breakthrough in reducing the impact of time-consuming tasks such as RTL, post-synthesis and timing simulation, logic synthesis and implementation.

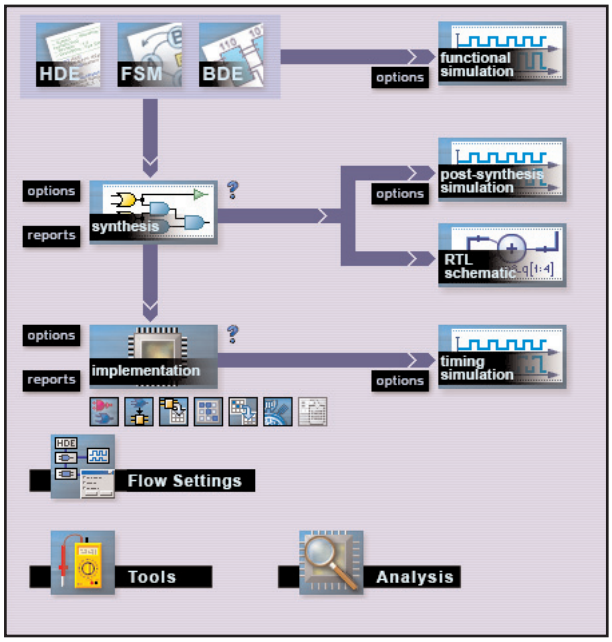


BENEFITS

- One integrated design flow for FPGA and PCB design
- No more manual creation of a matching description of the FPGA to use in the PCB design or physical design
- Vendor independent FPGA design flow manager allows integrating and running any synthesis and implementation tool
- Graphical design entry tools mixed VHDL and Verilog simulation and verification, project management
- Strict adherence to latest IEEE language standard
- Bring products to the market faster
- Easy adoption of FPGA technology in the product design
- Maintain competitive flexibility late into the design cycle
- Explore new manufacturing and assembly efficiencies
- Enhance product quality

ZUKEN

The team-based approach of complex designs and the integration with the PCB design allow them to dramatically improve their productivity, minimize the impact of late-cycle design change and to control the whole design cycle accurately.



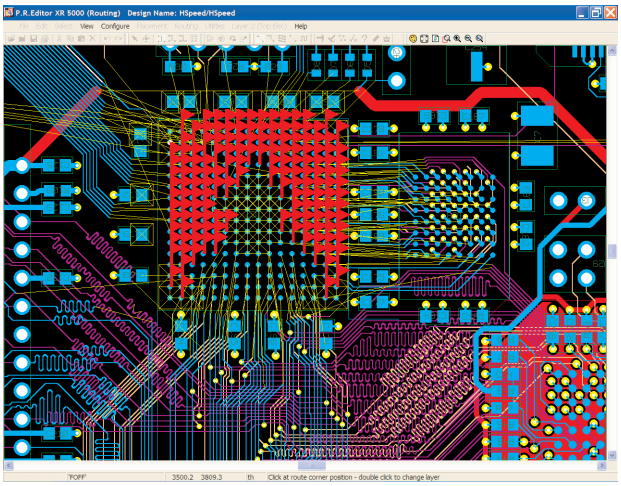
CADSTAR FPGA offers:

Vendor independent Design Flow Manager

An integrated environment that offers text and graphical ways of design entry, ability to run RTL, post-synthesis and timing simulation, ability to verify the design using rich set of debugging tools, integrates and runs any combination of logic synthesis and implementation tools thus offering a robust and complete FPGA design and verification, allows easy single-click export and import of I/O Pin information between FPGA and PCB design thus dramatically reducing manual, time-consuming data entry and verification to ensure pin synchronization of both environments.

Design Entry Tools

A variety of design entry tools such as advanced HDL editor, Finite State Machine (FSM) editor, Block Diagram Editor (BDE) are available that allow input of VHDL or Verilog HDL code. These easy-to-use graphical editors also support mixed HDL designs and can import almost any legacy design, even those made with another editor.



FPGA/BGA design in CADSTAR

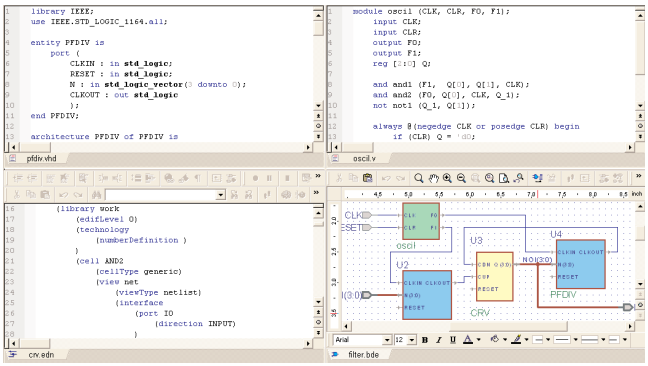
-Hardware Description Language Editor (HDE)
- -Actions recorder for often repeated operations
- -Automatic structure generation
- -Built-in customizable Language Assistant
- -Column selection & source code auto-formatting

-Block Diagram Editor (BDE)
- -Bottom-up and top-down design methodology
- -Multi-page hierarchical block diagrams
- -Mixed HDL design handling
- -Outputs VHDL or Verilog

-Final State Machine Editor (FSM)
- -Multiple state machines on a single diagram
- -Full-Moore and Mealy machines support
- -Outputs VHDL or Verilog

Mixed VHDL/Verilog Simulation

Ability to execute single language or mixed VHDL and Verilog Simulation at RTL, post-synthesis and timing levels. Allows executing simulation from the GUI or console window with help of DO, Tcl/Tk and Perl scripts.

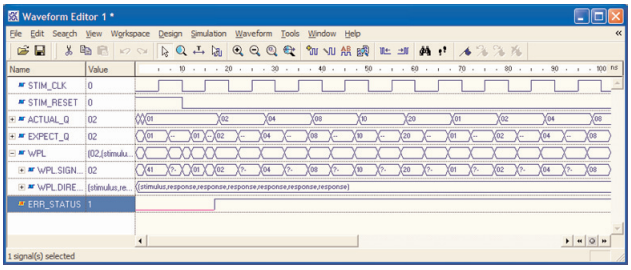


Multiple language support

Debugging

Any FPGA design that needs to be verified needs to have a powerful debugging environment. CADSTAR FPGA has a versatile debugging environment that makes debugging easy, versatile and intuitive. This is achieved by the high level of integration that CADSTAR FPGA provides between the design entry tools, simulator and debugging tools. The superior error navigation, advanced breakpoint management, graphical finite state machine debugging, probes highlighting values of nets/buses/signals/ports on Block Diagram Editor and the availability to use pre-defined stimulators (Clock, Formula, Value etc.) provide the ideal design environment to debug the HDL source code of the FPGA design.

Code Execution Tracing - allows step simulation of the design
Advanced Breakpoint Management- allows setting breakpoints on HDL code and on signal events/transactions/values that causes suspension of simulation
Watch Window - displays values of specific objects (signals, variables, nets, registers, etc.) in the simulated model
Call Stack Window - displays a list of subprograms being executed in the currently executed process
Processes View - displays a list of processes in the elaborated model along with their current status
List Viewer - displays values of selected signals and/or nets for all the assignments in the timing queue (time, event) in a tabled text format
Standard Waveform Viewer - displays simulation results in the form of graphical waveforms
Follow Object - allows users to follow objects in the simulated design. Follow object can be used in HDL editor, Block Diagram Editor and Finite State Machine Editor, watch window, processes view and standard Waveform viewer



Waveform Editor

Logic Synthesis

Logic synthesis is performed based on a set of user defined constraints that optimize the RTL design into equivalent blocks consisting of flip flops, logic gates, etc. The results of logic synthesis produce an FPGA netlist that can be passed to the appropriate vendor's place and route tool. CADSTAR FPGA offers direct interface to all popular logic synthesis tools and vendor place and route tools. All design information is passed from one tool to the next and managed by CADSTAR FPGA.

Supported synthesis tools include Synplify Pro, OEM editions of Synplify, Xilinx XST, Altera QuartusII Synthesis, Precision RTL Synthesis, Leonardo Spectrum, Synopsys FPGA Compiler II, Synopsys FPGA Express. After successful completion of synthesis, post-synthesis HDL files/netlist is generated which can be used for post-synthesis simulation and for implementation of the design.

Post-Synthesis Simulation

CADSTAR FPGA will accept the post-synthesis HDL files/ netlist produced by logic synthesis to assure that the functionality of the FPGA design was not lost during logic synthesis. Post-synthesis simulation can be done to simulate and verify the functionality of the design. By using the netlist that will also be used by the FPGA vendor's place and route tool, you will be confident that your functionality still remains.

Implementation

FPGA implementation can be run for Actel, Altera, Lattice, Quicklogic and Xilinx. At this stage, FPGA I/O pin assignments (I/O Constraints) are placed in order to optimize the place and route of the design. A constraints file is included and implementation is run for any FPGA vendor. After successful place and route of the design, back-annotated timing netlist and the SDF files are generated for timing simulation. Also an FPGA pin information file is generated which can then be exported to CADSTAR PCB design editor with a single click.

Timing Simulation

Timing simulation is a very important step in making sure that the FPGA device's functionality meets all required timing requirements for the design. Since CADSTAR FPGA comes with all FPGA vendor libraries pre-compiled, the software is ready to simulate the worst-case place and route timing delays by using the VHDL or Verilog netlist with the SDF (Standard Delay Format) file.

Why FPGA Pinout Changes

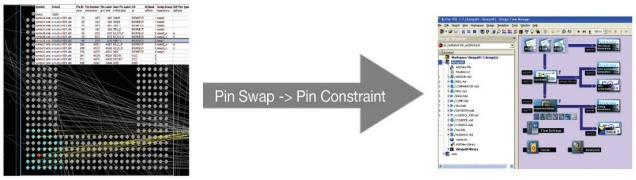
There are strong reasons for changes in FPGA pinout throughout the system design process. There are many areas where changes might occur.

-Pinout changes because of design constraints. With today's highly competitive and constantly evolving electronic markets, it has become critical for companies to shorten design cycles. The system architect defines an initial list of interface characteristics, which FPGA and PCB designers use to start their design. This assignment is later refined as both FPGA and PCB teams progress with product development. Additionally, market changes throughout the development cycle may require changes to the pinout, such as adding support for a new protocol or adding a feature at the last minute.
-Pinout changes because of PCB constraints such as form-factor restrictions or board cost control. In these situations using the programmability and flexibility of the FPGA pinout can help solve PCB congestion or routing problems.
-Swapping pins to untangle nets on the board. This reduces the number of vias needed and may reduce the number of layers. This helps in improving signal integrity and electromagnetic emissions.
-Adjusting I/O property to augment board signal integrity by lowering the signal drive strength or slew rate.
-Pinout changes because of FPGA constraints. These pinout changes are because of:

-Timing. Margins on some signals going into or out of the device may be tight enough that only a limited set of package pins will work.
-Dedicated/special-purpose pins. Because only a subset of package pins can be programmed to function as special-purpose pins (such as global or regional clocks or programming pins), this places constraints on the board to route signals to these capable I/Os.
-Voltage/termination compatibility. FPGA I/Os are grouped in banks, with all pins in a particular bank sharing power and reference voltages. This means that once a particular voltage is used in this bank, only I/Os with compatible voltage can be assigned in the same bank. This may force to select pins on the FPGA package that are not optimal from a PCB routing standpoint.

CADSTAR FPGA I/O Synchronization

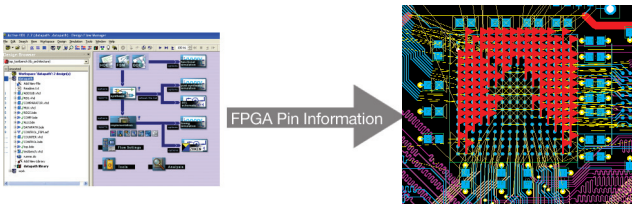
Because of the reasons described above (Why FPGA Pinout changes) a strong and robust I/O synchronization interface is necessary and that is exactly what CADSTAR FPGA provides by easy single click export/import of pin information files between FPGA and PCB design environments facilitating I/O synchronization.



Pin Synchronisation

Export of FPGA Pin information file to CADSTAR PCB Design Editor

With a single click feature FPGA pin information file (after implementation of the design) is exported to CADSTAR PCB Design Editor in the CSV file format. CADSTAR FPGA creates FPGA symbols for the PCB design and manages any interface changes between the FPGA and PCB design process. PCB design runs in parallel with FPGA design. PCB component are created to use the FPGA in the PCB design process. This is done easily in CADSTAR by using the PCB Component BGA Wizard. Schematic symbols can be created in CADSTAR by using the schematic symbol block wizard. The CADSTAR library editor can be used to rapidly build the complete part required for SCM & PCB design



Pin Export to CADSTAR

Gate/Pin swaps with CADSTAR P.R.Editor

P.R.Editor XR (Place & Route) and *P.R.Editor XR HS* combine placement and routing using advanced interactive placement tools, including component push-aside and spring-back functions, and optimum and legal position indicators, giving the user the ultimate control over component placement.

For optimum place and route of the PCB design - pin swapping is required. Pin swap in PCB requires an updated file (CSV format) to be sent back to FPGA design environment in CADSTAR FPGA to update the FPGA implementation

Import of Pin Swap file to FPGA design environment

CADSTAR FPGA imports Pin I/O file in CSV format from CADSTAR (containing pin swaps and/or renames) and generates a new constraints file for the FPGA place and route tool to update the FPGA. The required synthesis and place and route tools are again run from within the CADSTAR FPGA design flow manager thus updating the Silicon with respect to PCB design changes.

Active-HDL Configuration (CADSTAR FPGA)

Feature	Configuration
Design Management	
Design Browser	_
Support for Multi-Design Workspace	Single Workspace
Design Flow Manager for All FPGA Vendors	_
Workspace and Design Archiving	_
Design Entry	
HDL and Text Editor	_
Language Assistant with Templates and Auto-complete	_
State Machine Editor	_
Block Diagram Editor	_
Hierarchy Viewer with Configurations Support	_
Pre-compiled Vendor Libraries	_
CADSTAR Import/Export - Pin list	_
Simulation	
VHDL Simulation	Lite
Verilog® HDL Simulation	Lite
Mixed VHDL/Verilog Simulation	Lite
Verilog Programming Interfaces (PLI/VPI)	_
Value Change Dump (VCD and Extended VCD) Support	_
Simulation Model Protection/Library Encryption	_
Library Refresh	_
Debug	
Code Execution Tracing	_
Advanced Breakpoint Management	_
Standard Waveform Viewer/Editor	Viewer Only (.awf)
List Viewer	_
Watch	_
Call Stack	_
Processes View	_
Follow Object	_
Other	
Tcl/Tk and Perl Scripting	_
Licensing	
Node Locked License	_
Floating License	_

CADSTAR FPGA – Simulation Limitations

Slow down compared to full commercial release

- 6x (up to 2,000 instances)
- 20x (2,001 and 10,000 instances)
- 1% above 10,000 instances

Simulation runtime limited to

- 2ms

Pin List - unlimited number of pins